CLAIMS

What is claimed is:

1. A MOS transistor formed in a silicon substrate comprising: an active area surrounded by an insulating wall;

a first conductive strip covering a central strip of the active area;

a second conductive strip placed in the active area right below the first conductive strip; and

conductive regions placed in two recesses of the insulating wall and placed against ends of the first and second conductive strips, wherein, the silicon surfaces of the active area opposite to the conductive strips and conductive regions are covered with an insulator forming a gate oxide.

2. The transistor of claim 1 wherein the first and second conductive strips are made of polysilicon and the insulating wall is made of silicon oxide.

3. The transistor of claim 1 with two conductive strips, wherein the conductive regions placed against the first and second strips are separate.

4. A method for forming a MOS transistor, comprising the steps of:

forming at a periphery of an active area of a silicon substrate an insulating wall protruding from the substrate surface;

forming in the active area a stack of layer pairs, each pair comprising a single-crystal silicon layer and a layer of a material selectively etchable with respect to silicon;

forming a strip of a material selectively etchable with respect to silicon above the stack and the insulating walls, the strip substantially extending above a central strip of the active area;

anisotropically etching the stack on either side of the strip;

growing silicon by epitaxy;

forming a protection layer of a material different from that of the strip, of the insulating walls, and of the stack;

disengaging and removing said strip;

etching the insulating walls unprotected by said protection layer at least down to a bottom of the stack;

removing the stack layers made of a material selectively etchable with respect to silicon;

forming a thin silicon oxide layer at the surface of the silicon areas; and

filling with a first conductive material.

5. The method of claim 4, comprising between the step of growing silicon by epitaxy and the step of forming a protection layer a step of doping the silicon on either side of the remaining portion of the stack.

6. The method of claim 4, comprising, prior to the step of growing silicon by epitaxy, a step of doping the ends of the remaining portions of the silicon layers of the stack.

7. The method of claim 4, comprising prior to the step of forming a protection layer, a silicide-forming step.

8. The method of claim 4, further comprising the steps of:

etching said first conductive material to expose a silicon oxide portion covering the upper part of the active area;

removing said silicon oxide portion;

forming an insulating layer above said conductive material and the upper part of the active area;

filling with a second conductive material.

9. The MOS transistor of claim 1 wherein the second conductive strip is one of a plurality of second conductive strips, said second conductive strips together with said first conductive strips forming a stack.

10. The MOS transistor of claim 9 wherein the number of second conductive strips is 1, 2 or 3.

11. The MOS transistor of claim 10 wherein each said conductive strip of said stack is separated from one another by a silicon layer.12. A MOS transistor formed in a silicon substrate comprising:

an active area surrounded by an insulating wall;

first conductive strip covering a central strip of the active area and forming first gate;

a first insulating layer immediately below said first conductive strip;

a second conductive strip placed in the active area below said first insulating layer and separated therefrom by a single-crystal silicon layer; and

conductive regions below first insulating layer, said conductive regions being placed in two recesses of the insulating wall and against ends of the second conductive strips and said silicon layer, said conductive regions and said second conductive strip forming second gate, wherein, the silicon surfaces of said active area facing said second conductive strip and conductive regions are covered with a second insulating layer.

12. The MOS transistor of claim 11 wherein said first conductive strip is made of polysilicon.

13. The MOS transistor of claim 11 wherein said first conductive strip is made of aluminum.

14. The MOS transistor of claim 11 wherein said second conductive strip and said conductive regions are made of polysilicon.

15. The MOS transistor of claim 11 wherein said first and second insulating layers are silicon oxide.